Hardware Simulator for MIMO Radio Channels: Design and Features of the Digital Block

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Abstract – This paper presents the realization of the digital block of a hardware simulator of MIMO propagation channels for UMTS and WLAN applications. The hardware simulator must reproduce the behavior of the radio propagation channel, thus making it possible to test "on table" the mobile radio equipments. The advantages are: low cost, short test duration, possibility to ensure the same test conditions in order to compare the performance of various equipments. After the presentation of the general characteristics of the hardware simulator, an architecture of the digital block is proposed and its accuracy is analyzed.

I. Introduction

The UMTS (Universal Mobile Telecommunications System) and WLAN (Wireless Local Area Network) tele-communication systems of third generation and beyond are able to offer to general public high-rate multi-media services. MIMO (Multiple-Input Multiple-Output) systems make use of antenna arrays at both sides of a radio link to drastically improve the capacity over more traditional systems.

However, the transmitted electromagnetic waves interact with the propagation environment (indoor/outdoor). It is thus necessary to take into account the main propagation parameters during the design of the future communication systems. The optimal choice of the modulation, coding, etc. for these communication systems is based on a reliable model of the radio propagation channel. Moreover, after the realization of a communication system, its experimental performance can be evaluated by using a hardware radio channel simulator. A hardware simulator can also be used to compare the performance of various radio communication systems in a time-variant propagation channel in the same test conditions. On the market, there are some hardware channel simulators: Propsim [1], Smartsim [2], Spirent [3], but they are very expensive and therefore prohibitive for a communication laboratory.

This paper presents the design of the digital block of a hardware simulator for indoor/outdoor MIMO radio channels. Section II of the paper deals with the architecture of the digital block of the hardware simulator. This section is divided into two parts: General Characteristics and Digital Block describing the proposed architecture and several parameters useful to design the hardware simulator. In Section III the accuracy of the digital block for the proposed architecture is analyzed. The prototyping platform and the first results are also described. Lastly, in Section IV, an accuracy improvement is described and new corresponding results are presented.

II. Hardware Simulator

A. General Characteristics

The simulator must reproduce the behavior of a MIMO propagation channel for indoor and outdoor environments. It must operate with RF signals (2 GHz for UMTS and 5 GHz for WLAN). In order to make adjacent channels interference tests for UMTS systems, it is useful to consider three successive channels with 5 MHz bandwidth. Therefore, the frequency bandwidths B are 15 MHz for UMTS and 20 MHz for WLAN.

Moreover, UMTS uses two operating modes: the TDD mode (Time Division Duplex) having the same frequency band for both uplink and downlink and the FDD mode (Frequency Division Duplex) having different frequency bands. In addition, depending on the strength of the transmitted signals, the simulator must be able to accept input signals with wide power range, between - 50 and 33 dBm, which implies a power control for the simulator inputs.

The design and the realization of the RF blocks for UMTS systems were completed in the previous SIMPAA (SImulateur Matériel de Propagation pour Antennes Adaptatives) project [4]. The RF blocks will need some modifications required by WLAN specifications. The objectives of the actual regional project SIMPAA2 mainly concern the channel model block and the digital block of the MIMO simulator, as shown in Fig. 1 by the gray blocks.

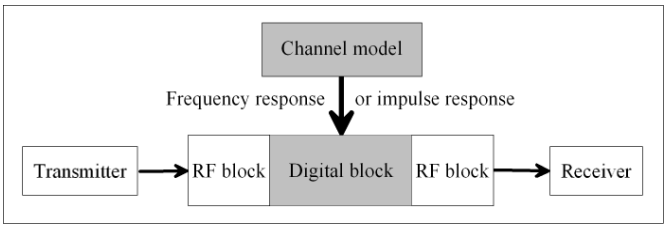

Figure 1: Block diagram of a one-way SISO channel.

The RF blocks have been described in [5]. For a one-way SISO (Single-Input Single-Output) channel, the first RF block realizes a frequency down-conversion. Its function is to obtain a real signal with a power spectrum within [0, B] frequency band to avoid complex computation and therefore to use less resources. The second RF block realizes the frequency up-conversion of the output signal.

The channel models used by the simulator are obtained from measurements by using a time domain MIMO channel sounder designed and realized at the IETR [6], as shown in Fig. 2.

Figure 2: MIMO channel sounder.

This MIMO channel sounder is based on the correlation technique [7]. For each SISO channel, the sounder gives the measured complex envelope of its impulse response. During the measurement of all SISO channels, the MIMO channel must be practically invariant. This limits the mobile speed and therefore the maximal value of the Doppler shift.

Each randomly time-variant SISO channel is described by one of the Bello's characteristic functions [8]. A simple way to use these measurement results is to compute, for each location of the mobile transmitter, the frequency responses $H_{i,j}(t,f)$ as Fourier transforms of the impulse responses $h_{i,j}(t,\tau)$ of the MIMO propagation channel. These frequency responses can be used to supply the "Channel model" block of each SISO channel, as shown in Fig. 1. Periodically, the frequency responses must be actualized, in order to simulate the channel time-evolution. The "refreshing" period of the frequency responses is determined by the channel coherence time, thus by the mobile speed and the propagation environment. As the number of the recorded files is finite, it will be necessary to periodically replay the whole set of frequency responses.

B. Digital Block

In order to obtain a suitable trade-off between complexity and latency, two solutions were considered: a time domain approach with FIR filters for indoor environments and a frequency domain approach with FFT/IFT modules for outdoor environments.

For outdoor environments, the channel impulse responses are longer, more samples are necessary to describe them. Therefore, computations are carried out in the frequency domain because FFT modules need fewer resources than FIR filters. The frequency domain architecture uses only one complex multiplication but needs one FFT module for each SISO channel and one IFT module for each receive antenna. These modules increase the latency of the digital block.

On the other hand, for indoor environments, the FFT and IFT modules have too much latency, therefore it is judicious to use FIR filters which perform convolutions. Several real multipliers are used, their number depends on the length of the channel impulse response.

Fig. 3 describes the architecture of the digital block for both frequency domain and time domain.

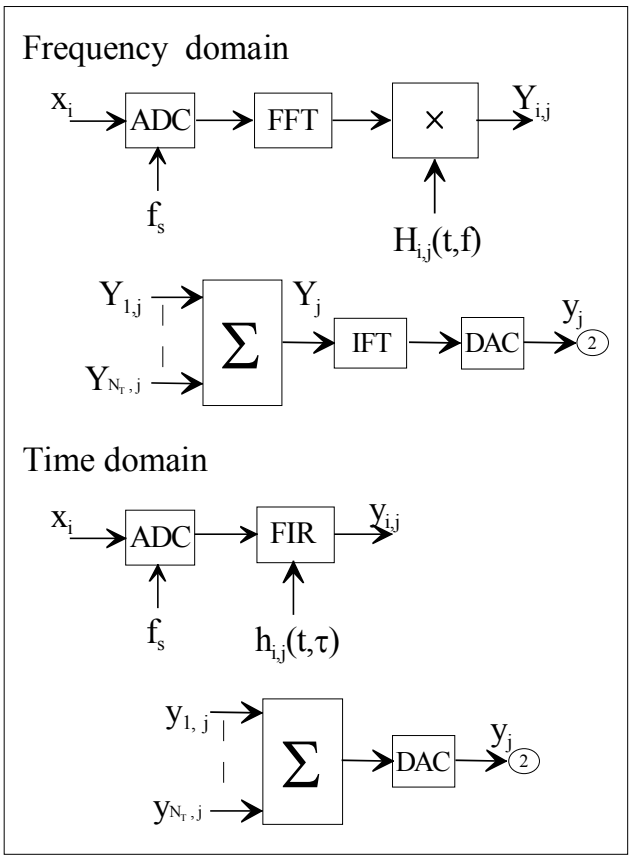

Figure 3: Digital Block.

For an outdoor environment, the digital block operates in the frequency domain. The Fourier transform of the input signal, obtained at the output of the FFT block, is multiplied by the channel frequency response $H_{ij}(t,f)$. The signal $Y_j(t,f)$ is the sum of the contributions of each SISO channel. This signal is truncated, depending on the number of bits of the input of the IFT block which gives the low-frequency output signal $y_j(t,\tau)$. After the D/A converter, the resulting signal represents the input of the up-conversion RF block.

For an indoor environment, the digital block operates in the time domain. The FIR filter computes the convolution product between the sampled input signal and the channel impulse response $h_{ij}(t,\tau)$. As for the frequency domain, the signal $y_j(t,\tau)$ of the j^{th} receive antenna is the sum of the SISO $y_{ij}(t,\tau)$ signals. Then, this sum must be truncated according to the number of bits of the D/A converter.

Based on Shannon theorem and the performance of the RF/IF filters, the sampling frequency f_s was chosen equal to 40 MHz for UMTS systems and 50 MHz for WLAN systems. This choice allows a reasonable low sampling rate and avoids the aliasing problems.

According to the considered propagation environments [7], Table 1 summarizes some useful parameters.

Table 1: Simulator parameters.

	Type	Cell Size	W_{teff}(µs)	N	W_t(µs)
UMTS (B = 15 MHz) (f_s = 40 MHz)	Rural	2-20 km	20	512	12.8
	Urban	0.4-2 km	3.7	128	3.2
	Indoor	20-400 m	0.7	28	0.7
WLAN (B = 20 MHz) (f_s = 50 MHz)	Office	40 m	0.39	20	0.4
	Indoor	50-150 m	0.73	37	0.74
	Outdoor	50-150 m	1.16	64	1.28

For these various environments, the length of the FIR filter or the FFT/IFT blocks is estimated by:

$$N_{eff} = \frac{W_{teff}}{T_s} = W_{teff}.f_s \qquad (1)$$

where W_{teff} is the width of the effective time window of the channel impulse response, i.e. the width of the time-interval where the impulse response can be considered not null. For outdoor environments, due to FFT/IFT blocks, N is the closest 2^n value of N_{eff}. The resulting $W_t = N.T_s$ value is also given in Table 1.

As the "streaming" mode of the FFT block does not obtain results similar to the theory, we only present the time domain solution, in this paper.

III. Implementation

A. Simulations

The adopted solution uses a prototyping platform based on 3 development boards (XtremeDSP Development Kit-IV for Virtex-4) from Xilinx [9], shown in Fig. 4. These boards will be installed within a computer, contrary to RF blocks placed in an external unit. A development board is built with a module containing the Virtex-4 SX35 programmable component chosen for its huge number of arithmetic blocks. Moreover, the XtremeDSP Development board provides a complete platform for high-performance signal processing applications.

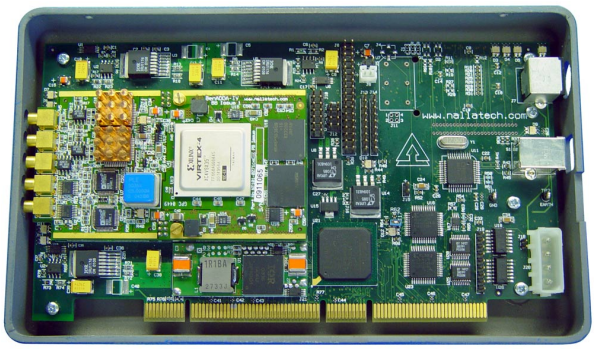

Figure 4: XtremeDSP Development board for Virtex-4.

This board features 2 high-performance ADCs (AD6645) and 2 DACs (AD9772A) with 14-bit resolution, a support for external clock, programmable clocks, two memory banks and interfacing via PCI or USB.

In order to determine the accuracy of the digital block, Gaussian signals are used: $x(t)$ is the input signal, $h(t)$ stands for the channel impulse response and $y(t)$ is the output signal. If $[-V_m,V_m]$ is the full scale of the converters, the $x(t)$ and $h(t)$ expressions are:

$$x(t) = x_m.\mathrm{e}^{\frac{-(t-m_x)^2}{2.\sigma_x^2}} \qquad (2)$$

$$h(t) = h_m.\mathrm{e}^{\frac{-(t-m_h)^2}{2.\sigma_h^2}} \qquad (3)$$

where $x_m = V_m/2$. The value of x_m must be chosen neither too small in order to obtain a good accuracy of the digitized signal, nor too big to avoid over-range values. The parameters of the test signals $x(t)$ and $h(t)$ are chosen in order to obtain the output signal:

$$y(t) = y_m.\mathrm{e}^{\frac{-(t-m_y)^2}{2.\sigma_y^2}} \qquad (4)$$

where: $y_m = \frac{V_m}{2}$, $m_y = \frac{W_t}{2}$, $\sigma_y = \frac{m_y}{4}$

Moreover, in order to obtain $y_m = x_m = V_m/2$, h_m is determined by:

$$y_m = x_m.h_m.\frac{\sigma_h.\sigma_x}{\sigma_y}.\sqrt{2\pi} \qquad (5)$$

where: $\sigma_y^2 = \sigma_x^2 + \sigma_h^2$

According to Table 1, the worst case obtained for WLAN environments needs a FIR filter with a length of 64. For the time domain, we have developed our own FIR filter, instead of using Xilinx MAC FIR filter because this filter does not allow reloading the FIR filter coefficients. According to the resolution of the A/D and D/A converters, the input and the output of this filter have a 14-bit resolution. The coefficients of the channel impulse response have a 16-bit resolution. The 64 coefficients are stored in the 32-block memory via the PCI bus, each block storing two coefficients. These coefficients are read at 100 MHz and the input data at 50 MHz. Thus, each FIR multiplier is used twice during two clock cycles of 100 MHz. The simulated chain is described on Fig. 5.

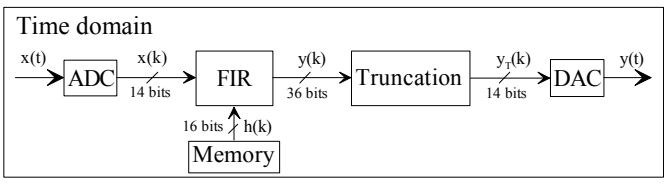

Figure 5: Time domain block diagram for a one-way SISO channel.

The output signal is presented in Fig.6. The simulation of this architecture is made with Xilinx tools and the results are

processed by MATLAB programs. There is an excellent agreement between Xilinx computed signals and the theoretical signal.

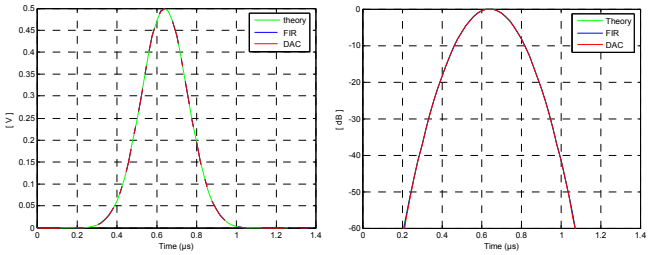

Figure 6: Time domain output signal in linear and log scale.

Fig. 7 shows the relative error and the SNR computed for the output signal.

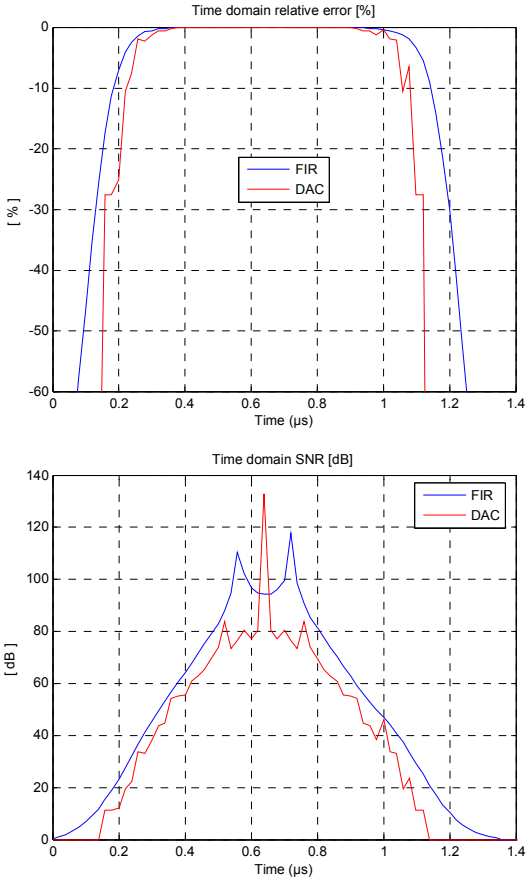

Figure 7: Time domain relative error and SNR for a one-way SISO channel.

If we compare Fig. 7 and Fig. 6 which represents the output voltage particularly in logarithmic scale, we observe that the greatest values of output voltage, i.e. values greater than - 40 dB relative to the maximum value of the voltage, have a relative error less than 1 % in absolute terms and a good SNR. The error can be much more important, but only for small values of the output voltage. The global values of the relative error ε and of the *SNR* of the output signal before and after the final truncation are computed by the following equations:

$$\varepsilon = \frac{||e||}{||y||}.100\ [\%] \tag{6}$$

$$SNR = 20.\log_{10}\frac{||y||}{||e||}\ \ [\text{dB}] \tag{7}$$

where y is the theoretical output signal, y_c is the computed signal (with or without truncation) and $e = y_c - y$.

For a given digital signal $x = [x_1, x_2, \ldots, x_N]$, $||x||$ is:

$$||x|| = \sqrt{\frac{1}{N}\sum_{k=1}^{N} x_k^2} \tag{8}$$

The results are ε = 0.0105 % and *SNR* = 79.56 dB without truncation. After 14-bit truncation, we obtain ε = 0.0305 % and *SNR* = 70.32 dB.

B. Synthesis

With Xilinx ISE and Modelsim software, it is possible to synthesize the chain for the time domain. As a development board has 2 ADC and 2 DAC, it can be connected to only 2 down-conversion RF units and 2 up-conversion RF units. Therefore, 4 FIR filters are needed to simulate a one-way 2 x 2 MIMO radio channel. For the time domain, the V4-SX35 utilization summary is given in the Table 2 for 4 FIR 64 with their additional circuits used to dynamically reload the coefficients of the FIR filters (i.e., the channel impulse response profiles). These coefficients are stored on the hard disk of the computer and read via the PCI bus. For 4 filters with 64 coefficients, the measured reloading time is 384.6 µs.

Table 2: Virtex-4 SX35 utilization for 4 FIR 64.

Number of Slices	7354 out of 15360	47 %
Number of logic LUTs	11318 out of 30720	36 %
Number of Block RAM	129 out of 192	67 %
Number of Flip Flops	9051 out of 30720	29 %
Number of DSP48s	128 out of 192	66 %

A FIR filter has 2 cycles of 32 multiplications and 5 addition cycles. One more cycle is necessary to add the results of each FIR. Thus, we have 8 cycles at 100 MHz, therefore 80 ns of latency for the digital block operation in the time domain. It is necessary to add approximately 38 ns of the ADC latency, and 17 ns of the DAC latency, according to their datasheets.

Moreover, for MIMO configurations with more Tx and Rx antennas, several boards connected together with point-to-point links must be used. Thus, the synchronization between these boards also needs one more clock cycle this time domain architecture.

In summary, the digital block and the converters have a latency of 135 ns for the time domain.

IV. ACCURACY IMPROVEMENT

For the weak values of the output signal, the relative error is great and the signal to noise ratio is less good. In order to improve the digital block, a new truncation algorithm is implemented. The main idea is to send to the digital inputs of the D/A converter the 14 most *effective* significant bits of the digital block output samples. If $n = [b_{N-1}b_{N-2}\ldots b_0]$ with $N > 14$ is the number to be truncated, then the truncated number is $n_T = [b_{k+13}b_{k+12}\ldots b_k]$, where k is the greatest positive integer for which $b_{k+13} = b_{N-1}$ and $b_{k+13} \neq b_{k+12}$. If the last condition is not verified (for small values of $|n|$), then $k = 0$ and the truncated number is $n_T = [b_{13}b_{12}\ldots b_0]$. In order to restore the correct values of the output signal, the number k becomes a new output used to compute the appropriate scale factor. Fig. 8 shows the new relative error and the SNR computed for the output signal. This new algorithm allows a very good agreement between Xilinx computed signals and the theoretical signal: the relative error is reduced and SNR is higher.

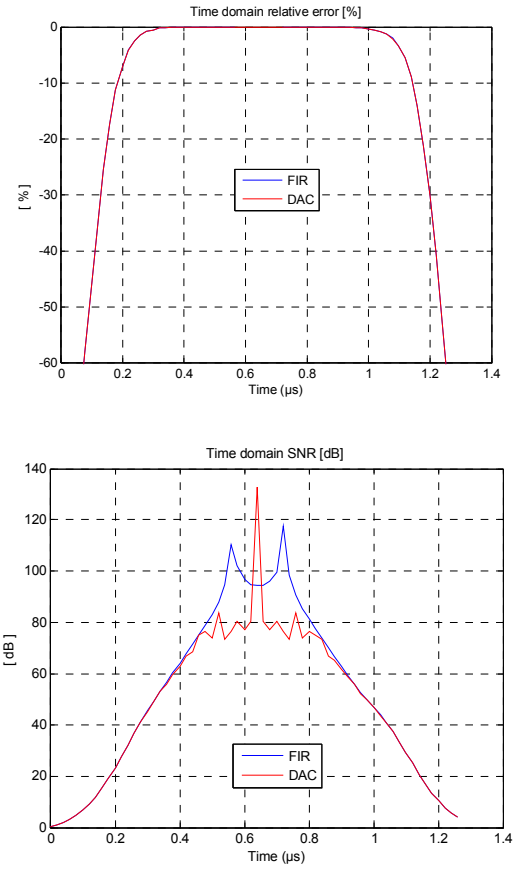

Figure 8: Time domain error and SNR for a SISO one-way channel.

After the new 14-bit truncation, the global values of the relative error and the SNR of the output signal are also computed by (6) and (7). The global value of the relative error is $\varepsilon = 0.0168$ % and the global value of the SNR becomes $SNR = 75.48$ dB. These values allow us to evaluate the accuracy improvement obtained with this new algorithm.

V. CONCLUSION

SIMPAA2 project has two main objectives. The first objective concerns the design and the realization of the digital block of the hardware simulator. The second objective concerns the MIMO channel models which must supply the digital block.

After a comparative study, in order to reduce the complexity and the latency of the digital block, the output signal of the MIMO simulator is computed in time domain for indoor environments. For this architecture, XILINX and MATLAB simulations were performed. The results obtained for a one-way SISO channel with the new truncation algorithm show an excellent accuracy of the output signal. However, this algorithm requires to compute a different scale factor for each sample of the output signal in order to obtain the correct values. This work continues with the design of the architecture for outdoor environments in order to reduce the latency of the digital block of the hardware simulator. Several solutions to reduce the "refreshing" period of the channel profiles are also considered.

Several measurement campaigns will be carried out with the MIMO channel sounder realized by IETR, for various types of environments (indoor, outdoor, penetration) and for both UMTS and WLAN frequency bands. The final objective of these measurements is to obtain realistic and reliable impulse responses of the MIMO channel in order to supply the digital block of the hardware simulator.

Lastly, the digital block of the MIMO hardware simulator will be implemented as a set of electronic boards placed within a computer. A Graphical User Interface (GUI) will be also developed to allow the user to configure the channel parameters: environment type, channel model, time window, mobile speed, etc.

ACKNOWLEDGMENT

The authors would like to thank the "Conseil régional de Bretagne" for its financial support of the SIMPAA2 project. Also, they thank Yvan Kokar for his helpful assistance.

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